Circuit Measures Small Currents Referenced To High-Voltage Rails

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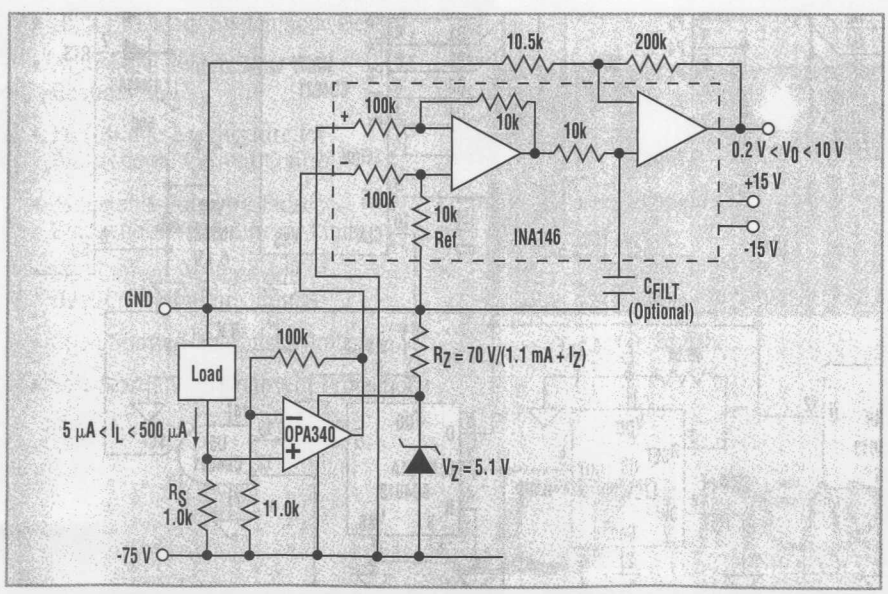
CIRCLE 520

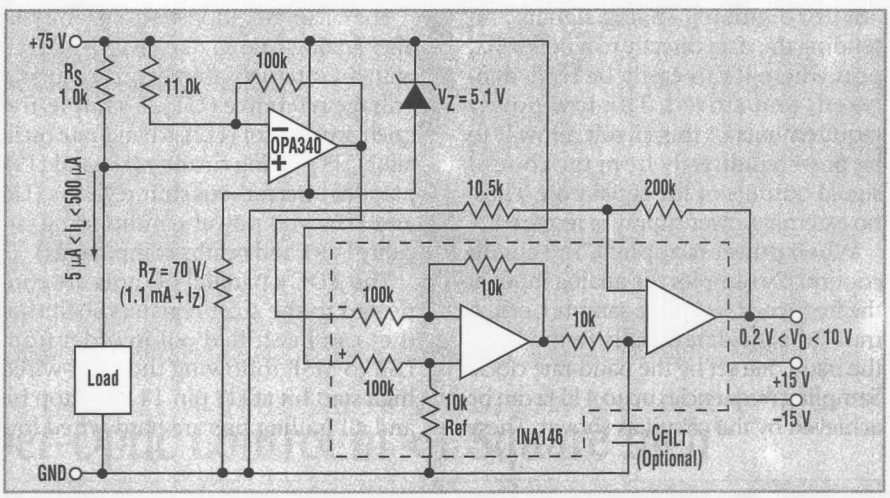
Designs that need to measure small signals riding on high-voltage power rails suggest the use of isolation devices. However, a high-common-mode-voltage instrumentation amplifier used with a rail-to-rail input and output amplifier can recover the signal cleanly and at a much lower cost.

Consider the system where a 5- to 500-μA current is flowing in a circuit at −75 V. A 1-kΩ sense resistor will not disturb the circuit in this instance and will provide a 5- to 500-mV signal. Direct application of the sense voltage to a difference amplifier is not advised because the magnitude of the sense resistor will unbalance the input of the difference amplifier. This will compromise the common-mode rejection of the difference amplifier. A solution is shown in Figure 1.

The voltage developed across the 1-kΩ sense resistor, R_S, is applied to the noninverting input of the OPA340. With a gain of 10, the output of the OPA340 swings from 50 mV to 5 V above the −75-V rail.



1. The sense voltage should be buffered using a CMOS op amp before sending the signal to the difference amplifier.



2. A similar circuit configuration will detect small currents referenced to a large positive voltage rail.

A simple zener-regulated 5.1-V supply is used to power the OPA340. This minimal regulator is adequate because the load current variation from minimum to maximum is 5 μA. This design is based on a load of 1.1 mA for the op amp and 5 mA for the zener diode. The value of R_Z is then set at (75 V − 5 V)/(6.1 mA) or 11.5 kΩ. Since the current through the zener is relatively constant, the change in supply for the op amp will be insignificant.

The INA146 is furnished with ±15-V supplies about ground. The input stage of the INA146 has a gain of 0.1 V/V. This gain ratio, accomplished with 100-kΩ input resistors, allows common-mode voltages of ±100 V. A gain of 20 V/V is set with the 200-kΩ and 10.5-kΩ second-stage gain resistors. The output signal will now swing between 0.2 V and 10 V.

Note that while the output signal is only positive, a negative supply is required for the INA146. This supply is necessary to allow the large negative

common-mode voltage.

Variations in the –75-V rail will cause the output of the OPA340 to change but will be rejected from the INA146 output by its common-mode rejection of 80 dB. This translates to 100 µV of output change per volt of change in the –75-V rail.

For the situation where the signal is sensed from a high positive supply, a similar circuit as shown in Figure 2 can be used.

Serial-Port-Powered ADC Streams Data To PC

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CIRCLE 521

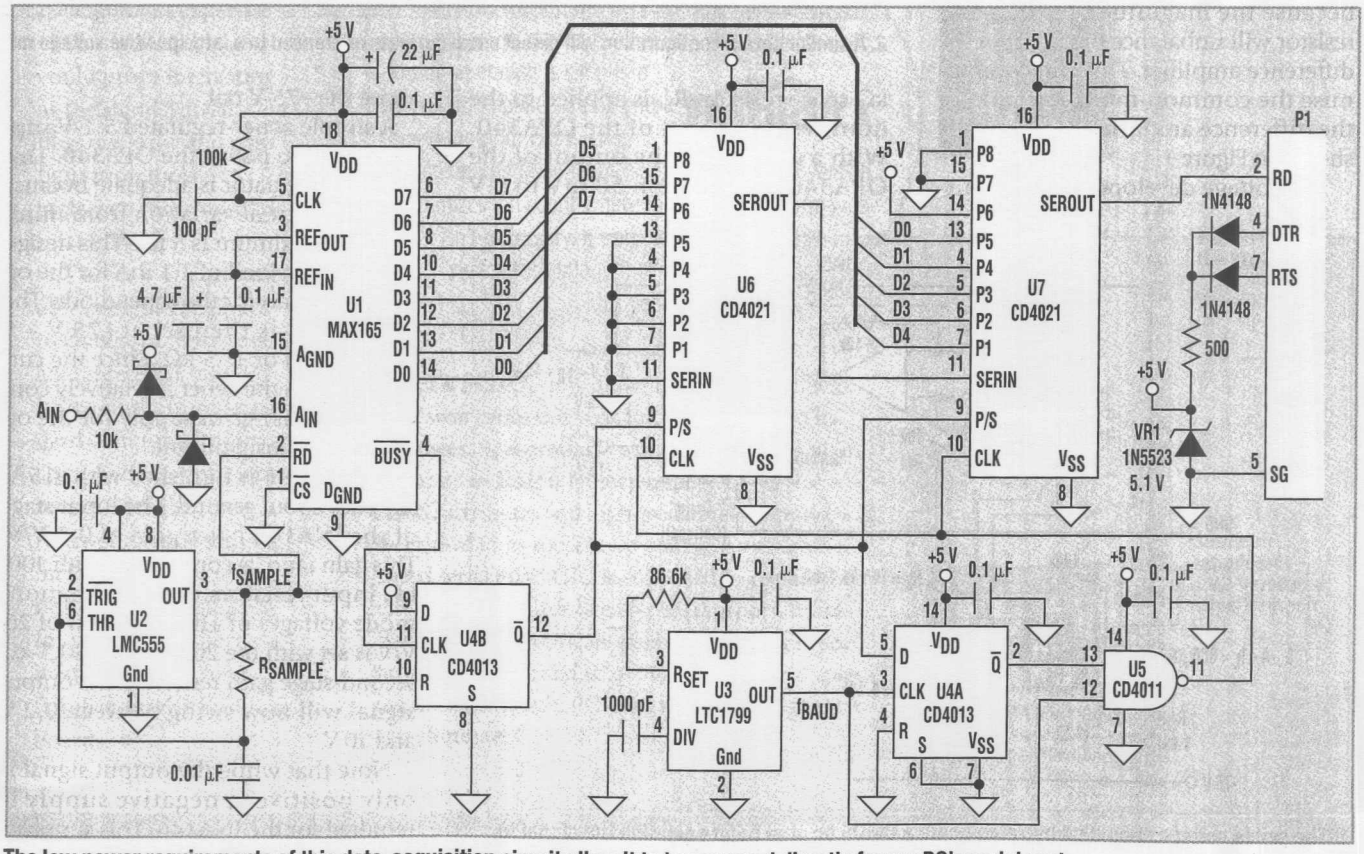
The circuit shown in Figure 1 provides a simple, low-power means of digitizing analog signals and sending the data directly to a PC's serial port where it can easily be read, analyzed, and stored. The low power requirements of this circuit allow it to be powered directly from the control signal outputs of the serial port. Thus, no external power supply is required.

When power is applied, the circuit continually samples the analog input at the frequency set by the sample clock. It transmits the data serially to the PC at the baud rate set by the baud-rate clock. Sampling frequencies up to 4 kHz can be achieved by the circuit as shown. These sampling rates make this circuit suitable for chart-recorder-type applications.

The circuit is comprised of an 8-bit parallel analog-to-digital converter (ADC) with an internal sample-and-hold and voltage reference (U1), a sample-frequency oscillator (U2), a baud-rate oscillator (U3), gating circuitry (U4 and U5), parallel-in/serial-out shift registers (U6 and U7), and power-conditioning circuitry (VR1 and nearby components).

The ADC's parallel outputs are connected to the shift registers such that they can be shifted out in order from LSB to MSB following the hard-wired high start bit at U7 pin 14. The stop bit and all trailing bits are hard-wired low (U6 pins 13, 4, 5, 6, 7, and 11, respectively) to complete the formatted serial byte with 8 data bits, no parity, and one stop bit. The serial output from this circuit at U7 pin 3 is a 0- to 5-V signal, which is adequate to be recognized as having pseudo-RS-232 logic levels by most PCs. The ASCII value of the eight data bits is inverted due to the RS-232 convention of a logic zero being a high-level voltage. This inversion can easily be corrected in the software used to read the data from the serial port.

U1 is the MAX165 CMOS-microprocessor-compatible, 5-µs, 8-bit, parallel-output ADC. The analog input voltage range is 0.0 to +2.46 V. U1 is



The low power requirements of this data-acquisition circuit allow it to be powered directly from a PC's serial port.